REMARKS

Applicant respectfully requests reconsideration of the present U.S. patent application. Claims 1 and 28 stand rejected under 35 U.S.C. § 102. Claims 2-17 and 29-33 stand rejected under 35 U.S.C. § 103. No claims have been amended, canceled or added. Therefore, claims 1-17 and 28-33 remain pending.

Claim Rejections - 35 U.S.C. § 102

Rejections of Claims 1 and 28 based on *Oikawa*

Claims 1 and 28 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,078,067 issued to Oikawa (*Oikawa*). For at least the reasons set forth below, Applicant submits that claims 1 and 28 are not anticipated by *Oikawa*.

Claim 1 recites the following:

> a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure, ...
> wherein the respective source and drain contacts of the D-mode FET and E-mode FET are coupled to the first layer, and the respective gate contacts of the D-mode FET and E-mode FET are coupled to the single barrier layer.

Claim and 28 recites similar limitations.

Oikawa discloses a device containing E-type and D-type FETs that is formed by sequentially growing on a semiconductor substrate a buffer layer, a channel layer, an electron supply layer, a third semiconductor layer, a second etching stopper layer, a second semiconductor layer, a first etching stopping layer, and a first semiconductor layer. See Abstract; Fig. 6; and col. 7, lines 45–65. *Oikawa* also discloses a device containing E-type and D-type FETs that is formed by sequentially growing on a semiconductor substrate a buffer layer, a channel layer, an electron supply layer, a threshold voltage control layer, an etching stopper layer, and a contact layer. See Fig. 3;

col. 2, line 62 – col. 3, line 6. In each of these devices, the gate electrode of the E-type FET is in contact with the electron supply layer, while the gate electrode of the D-type FET is in contact with the etching stopper layer. See col. 3, lines 6-10; and col. 8, lines 22-25.

Examiner contends that an etching stopper layer in *Oikawa* is the same as the barrier layer recited in claims 1 and 28. See Office Action, page 3, paragraph 4. Applicant neither agrees nor disagrees with the Examiner's contention with regard to the etching stopper layer in *Oikawa*, because it is not necessary to address that contention in order to refute the Examiner's 35 U.S.C. § 102 rejection. For the avoidance of doubt, Applicant is not saying that the etching stopper layer in *Oikawa* is the same as the barrier layer recited in claims 1 and 28, nor is Applicant saying that the etching stopper layer in *Oikawa* is different than the barrier layer recited in claims 1 and 28. While Applicant is not addressing such contention at this time, Applicant expressly reserves the right to address such contention in a future office action, if necessary.

Regardless of whether the Examiner is correct regarding the etching stopper layer in *Oikawa*, *Oikawa* does not disclose a D-mode FET and an E-mode FET in a multi-layer structure, wherein the respective source and drain contacts of the D-mode FET and E-mode FET are coupled to the first layer, and the respective gate contacts of the D-mode FET and E-mode FET are coupled to the single barrier layer. Thus, *Oikawa* fails to disclose at least one limitation of claims 1 and 28. Consequently, claims 1 and 28 are not anticipated by *Oikawa*. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 1 and 28 under 35 U.S.C. § 102.

Claim Rejections - 35 U.S.C. § 103

Rejections of Claims 2-17 and 29-33 based on *Oikawa* in view of *Lai*

Claims 2-17 and 29-33 were rejected under 35 U.S.C. § 103 as being unpatentable over *Oikawa* in view of U.S. Patent No. 6,452,221 issued to Lai et al. (*Lai*). For at least the reasons set forth below, Applicant submits that claims 2-17 and 29-33 are not rendered obvious by *Oikawa* in view of *Lai*.

Claim 7 recites the following:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure, ...

wherein the gate contact of the D-mode FET is coupled to the first layer, and a solid state amorphization region is beneath the D-mode gate contact within the first layer.

Claim 12 recites a similar limitation, in that the gate contact of the D-mode FET is coupled to one of the first layer and the single barrier layer.

Applicant agrees with the Examiner that *Oikawa* fails to disclose the limitations of claims 2-17 and 29-33. See Office Action, pages 5-13. However, Examiner contends that *Oikawa* in view of *Lai* discloses the limitations of claims 2-17 and 29-33. Examiner also contends that an etching stopper layer in *Oikawa* is the same as the barrier layer recited in claims 2-17 and 29-33. Applicant neither agrees nor disagrees with the Examiner's contention with regard to the etching stopper layer in *Oikawa*, because it is not necessary to address that contention in order to refute the Examiner's 35 U.S.C. § 103 rejections. For the avoidance of doubt, Applicant is not saying that the etching stopper layer in *Oikawa* is the same as the barrier layer recited in claims 2-17 and 29-33, nor is Applicant saying that the etching stopper layer in *Oikawa* is different than the barrier layer recited in claims 2-17 and 29-33. While Applicant is not addressing such contention at this time, Applicant expressly reserves the right to address such contention in a future office action, if necessary.

As explained above, *Oikawa* discloses devices in which the gate electrode of the E-type FET is in contact with the electron supply layer, while the gate electrode of the D-type FET is in contact with the etching stopper layer, and does not disclose a D-mode FET and an E-mode FET in a multi-layer structure, wherein the respective source and drain contacts of the D-mode FET and E-mode FET are coupled to the first layer, and the respective gate contacts of the D-mode FET and E-mode FET are coupled to the single barrier layer, as recited in claims 1 and 28. Similarly, *Oikawa* does not disclose a D-mode FET and an E-mode FET in a multi-layer structure, wherein the gate contact of the D-mode FET is coupled to the first layer, as recited in claim 7, or a D-mode FET and an E-mode FET in a multi-layer structure, wherein the gate contact of the D-mode FET is coupled to one of the first layer and the single barrier layer, as recited in claim 12. Thus, *Oikawa* also fails to disclose at least one limitation of claims 7 and 12.

Lai discloses an enhancement mode FET device that provides a Schottky barrier to inhibit undesirable surface depletion effects. See col. 1, lines 55-68. Applicant does not necessarily agree with Examiner's interpretation of *Lai* as set forth in the Office Action and may choose to address such interpretation in response to other office actions, if necessary. However, regardless of whether the Examiner's interpretation of *Lai* is correct, Examiner does not assert that *Lai* discloses a D-mode FET and an E-mode FET in a multi-layer structure, wherein the respective gate contacts of the D-mode FET and E-mode FET are coupled to the single barrier layer, as recited in claims 1 and 28; a D-mode FET and an E-mode FET in a multi-layer structure, wherein the gate contact of the D-mode FET is coupled to the first layer, as recited in claim 7; or a D-mode FET and an E-mode FET in a multi-layer structure, wherein the gate contact of the D-mode FET is coupled to one of the first layer and the single barrier layer, as recited in claim 12.

In fact, *Lai* does not disclose a D-mode FET on any layer of a multilayer device. *Lai* does not even disclose a D-mode FET, other than to say that D-mode FETs are disadvantageous because they "require an additional negative potential applied to the gate terminal for operation," and that they provide lower gain than E-mode FETs. See col. 1, lines 26-31. Therefore, not only does *Lai* fail to disclose a D-mode FET on any layer of a multilayer device, *Lai* would not be combined with *Oikawa* with regard to D-mode FETs, because *Lai* explicitly states that it does not apply to D-mode FETs.

Therefore, *Lai* fails to cure the deficiencies of *Oikawa* pointed out by Applicant. Thus, *Oikawa* in view of *Lai* fails to disclose at least one limitation of claims 1, 7, 12 and 28. Consequently, claims 1, 7, 12 and 28 are not rendered obvious by *Oikawa* view of *Lai* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claims 7 and 12 under 35 U.S.C. § 103.

Claims 2-6 depend from claim 1. Claims 8-11 depend from claim 7. Claims 13-17 depend from claim 12. Claims 29-33 depend from claim 28. Because dependent claims include the limitations of the claims from which they depend, Applicant submits that claims 2-6, 8-11, 13-17 and 29-33 are not rendered obvious by *Oikawa* in view of *Lai* for at least the reasons set forth above. Applicant therefore respectfully requests that the Examiner withdraw the rejections of claims 2-6, 8-11, 13-17 and 29-33 under 35 U.S.C. § 103.

CONCLUSION

For at least the foregoing reasons, Applicant submits that the rejections have been overcome. Therefore, claims 1-17 and 28-33 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the

undersigned by telephone if such contact would further the examination of the application.

Respectfully submitted,

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